The Digital Signal Processing Applications Newsletter

DSPatch

Number 36 Fall 1996

Analog Devices Delivers DSP Performance to Price-Sensitive Applications

In this issue

New Ultra-Low Cost DSP

With the new ADSP-2104 DSP, designers no longer must compromise performance to achieve low cost. The ADSP-2104 integrates 256 words of SRAM for data memory, 512 words of SRAM for program memory, two double-buffered serial ports (each with DMA, companding hardware and automatic data buffering; one with multichannel operation), a timer with prescaler, and a 20 MIPS 16-bit fixed-point core. The ADSP-2104's fixed-point core completes a 256-point FFT in 0.59 milliseconds, half as many cycles as the nearest competitor. The signal processing performance and level of integration found on the new DSP targets price-sensitive applications such as radar detectors, dictation machines, telephone answering machines, speakerphones, asynchronous motors, power meters, music synthesizers and toys. Packaged in a 68-pin PLCC, the ADSP-2104 is pin-compatible and code-compatible with the ADSP-2101, the ADSP-2105 and the ADSP-2115. Designers upgrading to these DSPs can add peripherals, memory or speed simply by plugging in a new DSP—no hardware changes are necessary. Priced at $4.50 in 100,000 unit quantities and $6.00 in quantities as low as 1,000 units, the ADSP-2104 is available now from Analog Devices and authorized distributors worldwide. For further system cost reduction, a ROM-based version is also available. The ADSP-2109 DSP features 4K words of customer-defined, factory-programmed on-chip ROM program memory, eliminating the need for an external EPROM in the system design.

Faster Speeds and Lower Prices Announced

Attracted by the high performance, easy-to-use algebraic assembly language and low-cost development tools, many designers have made the ADSP-2100 family their DSP of choice. Now, thanks to a new design, the popular ADSP-2101, ADSP-2105, and ADSP-2115 DSPs are available at lower prices, and with higher performance.

The devices have been redesigned for fabrication at ADI's foundry in Sinapore, Chartered Semiconductor. What's more, as part of the redesign the geometry was shrunk to 0.6 micron from 0.8, producing smaller, faster chips—and the cost savings is reflected in lower prices. The table on page 2 shows the changes in performance and price for the three devices.

Price (US $)	1k units	10k units	100k units	250k units
ADSP-2104KP-80 (5 volt)	$6.00	$5.25	$4.50	$4.30
ADSP-2104LKP-55 (3 volt)	$6.00	$5.25	$4.50	$4.30
ADSP-2109KP-80* (5 volt)	N/A	$9.00	$7.50	$7.50
ADSP-2109LKP-55* (3 volt)	N/A	$9.00	$7.50	$7.50

* ROM-version, minimum order quantity is 10,000 units

(continued on page 2)

ANALOG DEVICES

(continued from page 1)

More SPEED for Less Money

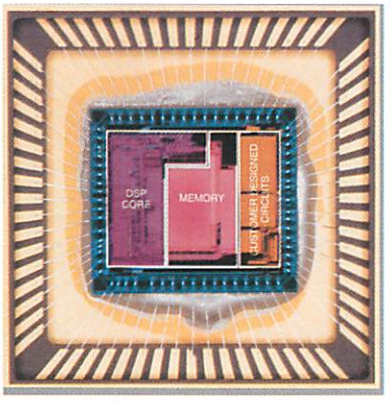
	Speed (MIPS)		Price (10,000 units)	
Product	Was	Now	Was	Now
ADSP-2101	20	25	$21.00	$19.90
ADSP-2115	20	25	$13.00	$11.00
ADSP-2105	13	20	$9.90	$9.50

Benchmarks

Instruction rate	20 MIPS (50 ns)	25 MIPS (40 ns)
Processor	ADSP-2105	ADSP-2115, -2101
FIR filter tap	50 ns	40 ns
Biquad IIR filter	350 ns	280 ns
LMS adaptive filter	100 ns	50 ns
1,024-point complex FFT	1.85 ms	1.48 ms
IS-54 VSELP	16.3 ms	13 ms
GSM speech coding	16.3% loading	13% loading
V.32bis modem	71% loading	57% loading
ADPCM (G.721)	38% loading	30% loading

Because the ADSP-2105, ADSP-2115, and ADSP-2101 are based on the ADSP-2100 family architecture, they are instruction-compatible. That means that you can start with the low-cost ADSP-2105 and migrate up to the ADSP-2115 and ADSP-2101 as your application demands without rewriting code. And because the three devices are each packaged in a 68-lead PLCC, you don't have to redesign your board. When moving up to the ADSP-2101, though, you'll most likely want to enhance your code to take advantage of its larger memory.

With 16-bit data words and 24-bit instructions and a high degree of parallelism, more operations can be done in a single cycle. Thus your algorithm can execute in less time. The benchmarks illustrate the performance of the ADSP-2100 family in several popular applications. ❖



The popular ADSP-21xx fixed-point core is now available for embedding in custom ICs.

ADI Puts Custom ASICs within Reach

Analog Devices has unveiled a unique, two-channel approach for making its ADSP-2Ixx 16-bit fixed-point DSP core widely available as an element for building application-specific integrated circuits (ASICs). One channel will be through Mentor Graphics, one of the world's leading vendors of electronic design automation tools. The other channel will be through Analog Devices, which is opening its ASIC DSP services to external customers.

Analog Devices has been developing and selling standard general-purpose and application-specific DSP chips for years. Application-specific standard products (ASSPs) with embedded 21xx DSP cores are being produced for a wide variety of applications in communications, audio, and motor control. Increasing numbers of external customers looking to migrate their designs to custom versions of the company's DSPs have prompted Analog Devices to launch its embedded DSP initiatives. What distinguishes Analog Devices' approach from that of other companies offering DSP cores as macro functions is the coupling of an architecture available in standard products on the merchant market with its open integration methodology. This methodology lets the OEM choose a road map to custom integration regardless of foundry or fabrication process.

The first cores are based on the ADSP-2171. The core includes all computational units and 2171 peripherals, except memory. Memory is configured to match the application. The core also includes new circuitry to enhance its testability with a minimum of external pins and provides in-circuit emulation capability. Future ADSP-21xx core options will include flexibility in peripheral selection and mixed-signal blocks.

(continued on page 3)

ASICs Through Mentor Graphics

By teaming with Mentor Graphics, Analog Devices gives you access to a unique channel that offers several benefits. Not only do you have the ability to embed a high-performance DSP architecture in your system-on-silicon designs, but you can select the level of design service, integration and fine-tuning you require to implement the architecture.

Working with Mentor Graphics' IC Technology Center (ICTC) through its Architecture-to-Silicon program, you can choose to have Mentor Graphics' engineers handle the integration of the core straight through any stage of the design process. Leveraging the ICTC's linchpin tools and design flow expertise lets you focus on your primary technology while distributing design costs and reducing time to market.

ASICs Through ADI

In addition to offering its DSP core through Mentor Graphics, Analog Devices has developed its own ASIC DSP design, integration, and fabrication services to carry products across successive design and manufacturing generations. To complement our DSP and mixed-signal expertise, Analog Devices has adopted ASPEC Technology's High Density Architecture (HDA) Design Implementation Technology (DIT), which includes process-optimized standard cell libraries and support for industry-standard EDA tools.

Analog Devices takes responsibility for integrating the ASIC design with the DSP core and memory. The customer provides the ASIC design to Analog Devices as a schematic for design by ADI, synthesizeable RTL, or a net list based upon Analog Devices' library files. An assembled, tested, and fully qualified device in the package of choice is delivered at the end of this process. Close working relationships between the customer and ADI and a rigorous review and approval process assure silicon that works the first time. ❖

World's Fastest Floating-Point DSP in Full Production

The most popular of Analog Devices' industry-leading SHARC DSPs, the ADSP-21062, which boasts 2 Mbits of dual-ported SRAM on chip, is now in full production, with lead times ranging from off-the-shelf delivery to a maximum of just ten weeks.

"With testing for high-grade commercial application conditions complete, we are executing a manufacturing plan that will provide a 500% increase in output for '97 versus '96," says David French, Vice President and General Manager for Analog Devices' Computer Products Division. "The SHARC product line continues to capture share in the rapidly developing market for floating-point DSP. We have made the manufacturing investment to support further growth of this business and achieve our goal of becoming the leader in floating-point DSP."

In addition to the 5V ADSP-21062, the SHARC family includes the ADSP-21060, with 4 Mbits of on-chip SRAM, and 3.3V versions of both the ADSP-21062 and the ADSP-21060. Industrial-temperature-range and military SMD versions are planned for later this year.

Price Reductions up to 20%

With the steep production ramp of the ADSP-21062, ADI has realized cost savings which are being passed on to customers. The 5V, 33MHz version is US $132.00 in 10ku. The 40MHz version is US $161.00.

Save $500 on Tools

From August 4th through November 1st, Analog Devices will be running a special offer on the SHARC EZ-KIT. Normally, US $1995, during this period the price will be reduced to US $1495. This unprecendented low price for floating-point development tools includes the EZ-LAB™ development board, compiler, linker, assembler, simulator, and runtime library. Call your local Analog Devices sales office or authorized distributor for information about these savings.

ADSP-21062 SHARC DSP

Benchmark	Performance
MFLOPS	120 MFLOPS
Instruction Execution Time	25 nsec
FFT, 1K Complex	0.46 msec
Divide, 32-bit Floating-Point	150 nsec, cycles
Vector Graphics	300,000 polygons/sec

Analog Devices to Build New Wafer Fab

Analog Devices recently entered into a joint venture with TSMC (Taiwan Semiconductor Manufacturing Company) of Hsinchu, Taiwan to build an 8" wafer fabrication facility in Camas, Washington, in the U.S. Northwest. Construction on the new venture, to be called WaferTech, began in July.

WaferTech will utilize the state-of-the-art process technology of 0.35 micron, shifting to 0.25 micron and eventually 0.18 micron.

Output from WaferTech will contribute to ADI's overall systems ICs capacity including its popular fixed-point (ADSP-21xx family) and SHARC floating-point DSPs.

According to Jerry Fishman, President of Analog Devices, "This is great news for our customers around the world. We have made major investments in our design, support, and manufacturing infrastructure that will meet or exceed their needs for the next several years." By 1999, the fab will output 30,000 wafers per month. ❖

Using DSP

Digital Signal Processing of Doppler Radar

by Richard L. Henderson
DSP Design Engineer
for Kustom Signals, Inc.

Traffic Safety Radar, based on the Doppler principle of a frequency shift proportional to speed, has been used by law enforcement officers for over 30 years. A traffic safety radar transmits a microwave frequency signal from a horn antenna and receives back the reflected waveform, which has been shifted proportional to the velocity of reflecting vehicle surface (the Doppler shift). The unit then uses a network of various self-tuning filters, automatic gain control and phase-locked loops to isolate, qualify and calculate the speed of the reflected surface or "target" if the radar is stationary, or both the patrol vehicle and the target vehicle if the patrol car is moving. At least that's how it used to be done.

The EAGLE series traffic safety radar, from Kustom Signals, Inc., using the Analog Devices' ADSP-2101, 16-bit, fixed-point DSP chip, has changed all of that. The EAGLE DSP uses a combination of time and frequency domain processing, as well as statistical and historical tracking algorithms, to process the Doppler return in all modes of operation, regardless of whether the patrol vehicle is stationary or moving.

The three frequency bands commonly used in traffic safety radar, X (10.525 GHz +/- 25 MHz), K (24.150 GHz +/- 100 MHz) and Ka (33.4 - 36.0 GHz +/- 100 MHz), all yield audio frequency Doppler shifts for vehicle speeds up to 210 MPH.

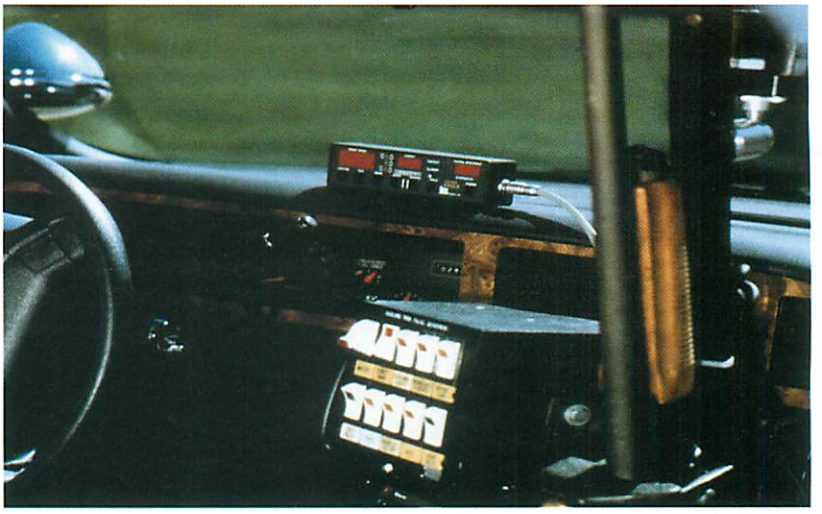
This made the ADSP-2101 an excellent choice for the processing requirements.

The ADSP-2101's processing bandwidth and clock speed were a very good match for processing the frequencies of interest. The assembly programming language and software development tools were powerful, yet straightforward to use. The dual serial ports provided a glueless interface to both the 8-bit coprocessor and the A/D converter. Also, given that all the audio filters, amplifiers, gain circuits and the phase-locked loop were replaced by the ADSP-2101, it made an excellent, cost-effective solution with the added benefit of significantly improved performance and reliability.

As a direct result of the ADSP-2101, the EAGLE has improved the effective range of traffic radar by up to 50%, depending on weather and traffic conditions. The EAGLE also has a reduced susceptibility to common interference conditions such as intermodulation distortion, fixed-frequency interference sources, compound Doppler frequency reflections and shifted speed returns due to large reflections from stationary objects such as large interstate traffic signs.

DSP has also allowed the EAGLE to incorporate functions not possible or cost-effective in traditional analog traffic safety radar. The EAGLE senses what frequency band antennae is connected and automatically configures for proper operation. It is capable of automatically performing a high-precision self-test automatically to ensure speed accuracy and to alert the operator of any malfunction. The unit is also capable of simultaneously tracking a strongest-reflected-target and a fastest-reflected-target while displaying both speeds identified as such. This is particularly useful in the scenario of a small sports car pulling out to pass a large, slow-moving vehicle like a semi-tractor trailer. The EAGLE can track and display the speeds of both vehicles, something impossible with traditional traffic radar.

The ADSP-2101 and DSP technology, combined with the power and flexibility of software based signal processing, have merged to form a significant advance in the area of traffic safety radar.



Improvements and enhancements are still being developed and can be added through software upgrades.

For more information, contact:

Kustom Signals, Inc.
9325 Pflumm
Lenexa, KS 66215-3347
Tel: (913) 492-1400
Fax: (913) 492-1703 ❖

Award-Winning Product Leverages SHARC DSP & Third Party Vendors

Continental Electronics Corp. of Dallas, Texas recently introduced a SHARC-based FM broadcast radio exciter. This was the first time a general-purpose DSP has been used to generate the "on air" signal for broadcast radio stations. The extensive support for the SHARC processor from third party vendors such as BittWare Research Systems and Hyperception reduced the time to market of this new product.

The Bytecast Series 802D Digital FM Exciter is a DSP based modulator for broadcast radio transmitters in the commercial FM band (88-108 MHz). It accepts program material such as music from either analog or digital sources. Using a cluster of 4 SHARC DSP chips the 802D converts and combines all the various program sources into a common format. The combined data stream is converted to a complex time domain signal in digital format. A specially designed card accepts this complex data from one of the SHARC Link Ports at a rate of nearly 2.5 million complex data points per second and converts it directly to the stations assigned carrier frequency.

Special requirements include high speed serial I/O for digital audio data and high speed ADCs. The high output rate requires interpolation of incoming data blocks to 16 times their original sample rate. Sufficient high speed SRAM is required to hold two of the interpolated blocks of data. As one is being fed to the external hardware another is being filled by the interpolation code. Because incoming data has up to 20 significant bits on two or more channels the use of floating-point math is required to avoid any loss of precision. This is a real-time application so maximizing I/O throughput is of great importance. Due to the volatile nature of government regulations governing broadcasting, future expansion capability is also required.

Given the above requirements, the SHARC is a natural choice. The availability of 2 Mbits of onboard SRAM satisfies the buffer requirements, so no external high speed memory is required. The high I/O bandwidth of both the serial ports and the link ports give ample capacity for future expansion. The DMA structure of the SHARC DSP allows all I/O transfers between SHARC DSPs and external hardware to be handled without any software intervention, thus leaving the DSP core free to do the required calculations. The ability to add multiple SHARC clusters allows future compute-intensive applications to be handled by a field upgrade.

For Continental Electronics, rapid prototyping of hardware and software algorithms was very important as there was a fixed deadline for a working unit. The SHARC processor is well supported by third party suppliers. For software prototyping and algorithm verification, Continental used Hypersignal for Windows® from Hyperception Inc.

BittWare Research Systems worked with Continental to custom design a four-SHARC DSP ISA card.

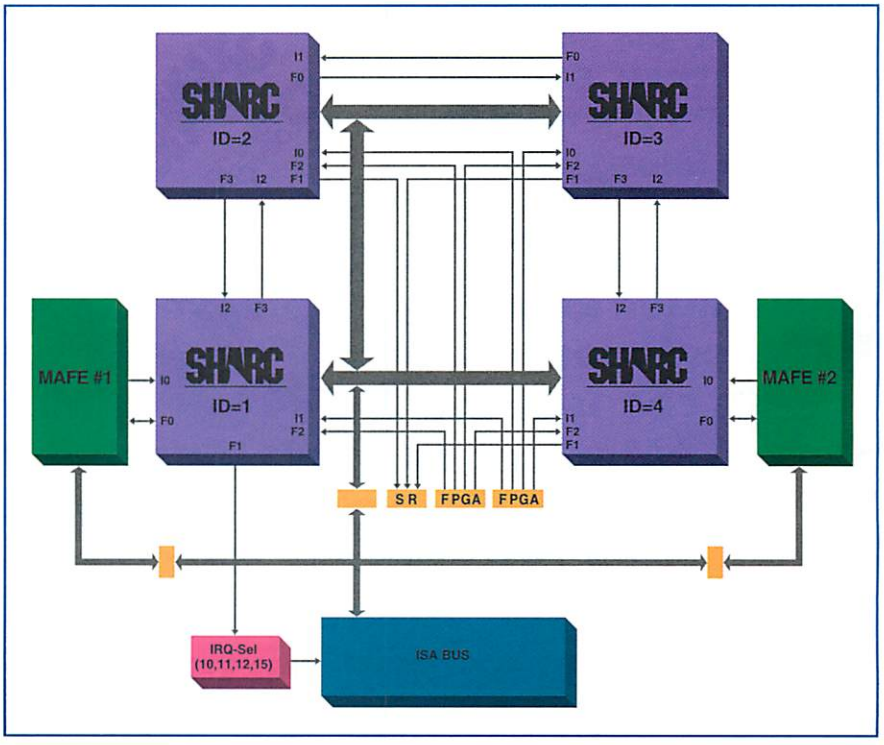
The first prototype cards worked exactly as envisioned, and software integration took one week.

The complete system was ready to demonstrate at the National Association of Broadcasters show in Las Vegas. The combination of DSP technology with numerous convenience features for the operator resulted in the 802D receiving the highest award for a new product.

For more information, contact:

BittWare Research Systems, Inc.
Tel: (603) 226-0404
Fax: (603) 226-6667
Internet: http:/www.bittware.com

Continental Electronics Corp.
P.O. Box 270879
Dallas, TX 75227-0879
Tel: 214-381-7161
Fax: 214-381-4949 ❖



Can Your High-Performance Design Survive A SHARC-Infested Market?

Succeed In Today's Competitive Waters With The World's Fastest Floating-Point DSP.

SHARC™ DSPs are populating just about every high-performance, math-intensive application – from arcade games, graphics workstations and image processing systems to digital audio broadcasting equipment, cellular basestations and LAN hardware. So to succeed in performance-hungry applications, join the leading OEMs. Design with SHARC.

Killer Price/Performance

With 40 MIPS/120 MFLOPS and non-intrusive DMA, SHARC delivers more performance per sq. in., per watt and per dollar than any other DSP. You can choose either 4 Mbits (ADSP-21060) or 2 Mbits (ADSP-21062) of dual ported SRAM on chip, eliminating slow off-chip memory accesses and bus bottlenecks, while reducing system size, power consumption and cost.

Benchmark	ADSP-21062 SHARC
MFLOPS	120 MFLOPS
Instruction Execution Time	25 nsec
FFT 1K Complex	0.46 msec
Divide 32-Bit Floating Point	150 nsec, 6 cycles
Vector Graphics	300,000 polygons/sec

Maximum Data Flow For All I/O Ports

SHARC offers 240 Mbytes/sec bandwidth over its external port and its six link ports, plus 40 Mbits/sec operation over two serial ports. Now you can move data in and out of the core fast enough to take advantage of its incredible speed. And an I/O processor provides non-intrusive DMA for all I/O ports.

Multiprocessing Dominance

A glueless external port connection to as many as six SHARCs and a host, plus six multiprocessing comm ports, distributed bus arbitration and a unified address space, make the SHARC DSP a "node-on-a-chip" for multiprocessing topologies.

SHARC PROCESSORS

3.3 Volts	5.0 Volts
4 M Bits SRAM	4 M Bits SRAM
40 MHz 33 MHz	40 MHz 33 MHz
2 M Bits SRAM	2 M Bits SRAM
40 MHz 33 MHz	40 MHz 33 MHz

Be on the look out for lower cost and higher performance chips, military and industrial versions as well as new, multichip modules. And our SHARC third parties can help you navigate the waters.

To order your SHARC EZ-KIT development system for a limited time, introductory price of just $1,495*, call 1-800-ANALOGD (262-5643)† or a distributor near you. For data sheets, dial AnalogFax™ at 1-800-446-6212, Faxcode # 1870. Or visit us on the World Wide Web.

Call 1-800-ANALOGD (262-5643)† for our $1,495* Special Tools Offer including: Development Board, Compiler, Assembler, Linker, Simulator and Run-Time Library.

http://www.analog.com

ANALOG DEVICES
Analog. Digital. Solutions.

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106.
Distribution, offices and application support available worldwide.

SHARC development tools are available from these authorized Analog Devices distributors:
Allied Electronics · Tel. 800-433-5700 · Bell Industries · Tel. 800-289-2355 ·
Future Electronics · Tel. 800-388-8731 · Hamilton Hallmark · Tel. 800-332-8638 · Newark Electronics · Tel. 800-463-9275 ·
Pioneer · Tel. 800-227-1693 · Wyle · Tel. 800-414-4144

* US dollars. Offer expires Nov. 1, 1996.

† Outside U.S., please call 617-461-3392.

DSP Apps

Program Code and Data Overlays in DSP Systems

Using a DSP that has large amounts of RAM on-chip, like the ADSP-2181, can reduce the chip count of your system by eliminating the need for external memory. If the memory requirements exceed the amount of memory on the DSP, you may still be able to eliminate external memory by reusing the DSP's RAM. This technique is known as overlaying.

In a DSP system, two types of overlays may be needed, code and data. Code overlays can be used where multiple tasks have to be performed at different times or one large task needs to be performed that can be partitioned in time. Data overlays can be used where multiple data sets must be processed using the same algorithm or large amounts of data must be processed on an ongoing basis.

ADSP-2181 Overlay Mechanisms

Overlays are effective only if the DSP has an efficient mechanism for transferring code and data. Of course, the transfer mechanism should have little or no impact on the DSP's execution of the algorithm.

The DMA capability of the ADSP-2181 provides two such mechanisms, a Byte DMA (BDMA) port and an Internal DMA (IDMA) port. The BDMA port allows the DSP to access up to 4 Mbytes of external 8-bit-wide memory such as EPROM or flash memory. The internal memory's contents can be loaded directly into the DSP's internal data or program memory. In addition, automatic byte unpacking allows the storage of 16-bit data and 24-bit instructions. The IDMA port is 16 bits wide, giving a host processor direct read/write access to the DSP's internal data or program memory.

Data Example

The ADDS-21xx EZ-KIT Lite development tool uses data overlays for its audio message, which is accompanied by music. Because the MPEG audio playback algorithm accesses 100 kbytes of compressed (encoded) data, which is larger than the data memory available on the ADSP-2181 (80 Kbytes), a low-cost EPROM is used for bulk data storage. For playback, data is continuously being overlaid into the DSP's memory so the decoding algorithm can process the data and output the samples. More specifically, the decoding algorithm works on one block of data while another block is loaded in its place from the EPROM, using the ADSP-2181's Byte DMA capability.

Code Example

Now, consider a common modem design consisting of a DSP data pump connected to a host processor. The host processor handles the data flow to and from the DSP and may also perform some compression and error correction tasks. The DSP performs all the data processing, as well as handling the telephone interface functions—DTMF dialing and detection, call progress detection, line condition determination, and the like. All of those tasks can require a lot of memory, but many of them need to be done only at discrete points in time. Using code overlays via the ADSP-2181's IDMA port, the modem code can be run from the DSP's internal RAM instead of external memory.

In summary, overlay memory techniques can significantly increase the efficiency of the DSP processor's on-chip RAM. ❖

Interfacing SHARC DSPs to Flash Memory

The memory initialization requirements of a SHARC multiprocessor system can be unusually large. For example, consider an image-processing application that requires a parallel-processing cluster of six SHARC DSPs. Each DSP is an independent processing element (PE) that is given a unique part of the task of processing video data in real-time. Each PE boots different code at power-up from a byte-wide nonvolatile memory. If ADSP-21062s are used, the total internal memory initialization requirements can approach 12 Mbits, and external memory requirements add to that amount. This storage can be implemented with flash memory without compromising field updatability and programming speed.

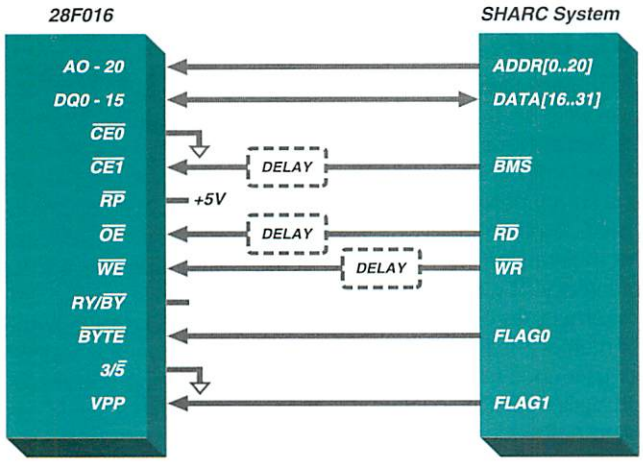
SHARC DSP to Flash Interface

Of the various electrically erasable nonvolatile memory products available, the 28Fxxx family is appealing to microprocessor system designers because of its very high storage capacities—up to 32 Mbits—and sophisticated microprocessor interface.

A 16-Mbit 28F016 easily services a multiprocessing cluster of six ADSP-21062s that use 12 Mbits and still have 4 Mbits to spare. This amount of memory would be needed if each SHARC DSP runs separate components of one application and requires access to external ROM data tables. One of the DSPs (the reset bus master) would have the ability to reprogram the flash with data it gets from a port or a host processor.

The interface between a SHARC cluster and a 28F016 flash device is shown in the block diagram.

Note that reconfiguration of the flash modes is possible during system operation. An optional way to



SHARC DSP to Flash Memory Interface

reconfigure the modes is to map an external latch into the SHARC DSP's external memory space and connect the outputs of the latch to the 28F016's mode selection inputs.

Interface Timing

Depending on the manufacturer and the speed of the flash memory, the interface timing varies slightly.

- Wait states may be needed, even though flash memories with access times of up to 65 ns are currently available. Wait states can be configured in the DSP's memory-mapped Wait register.
- An idle cycle is needed on read accesses if they are followed by accesses to external memory with fewer wait states, to allow enough time for the bus to reach high impedance. The time required to reach high impedance increases with increasing 28Fxxx access time.
- A hold cycle may be needed to meet the requirement for a data hold time or an address hold time from $\overline{WE}$. The hold cycle can be programmed using the DSP's Wait register to allow the data, address, and strobes to be held an additional cycle after a write is completed.
- The BMS signal may need to be delayed to meet the requirement for an address setup time to $\overline{CEx}$. The delay can be accomplished by passing the signal through a buffer having the required propagation delay.
- Similarly, the RD and WR signals may need to be delayed in the connection to the flash memory to meet an address setup requirement to $\overline{OE}$ and $\overline{WE}$.

Because only direct memory accesses assert the BMS pin, a SHARC DSP access to the flash must use DMA. To allow random ADSP-2106x core-driven accesses, external logic can selectively map the flash memory to the SHARC DSP's external memory space.

Interface Software Considerations

When data is read from the 28F016, the device behaves just like an EPROM: It drives data corresponding to the accessed address when $\overline{CE0}$, $\overline{CE1}$, and $\overline{OE}$ are enabled. For write or block erase operations, however, a command sequence is given to the 28F016, consisting of writes to the CUI to initiate an internal WSM algorithm. Based on the command sequence given, the appropriate WSM algorithm is used to generate internal control signals to the flash array to complete the desired operation. WSM feedback is accomplished through the $\overline{RY}/\overline{BY}$ line and the Compatible Status Register. Status information from the WSM includes erase operation success or failure, write operation success or failure, and Vpp level status.

To facilitate interactive communication between the SHARC DSP and the 28F016 during erase and write operations, a SHARC flash reprogrammer routine is needed. The routine initiates an erase or write operation and polls the CSR until it is completed. Then the routine tests bits in the CSR to make sure the operation has completed successfully.

Word transfers simplify the loader code for flash devices that support word accesses. The loader routine can reside in a read-only block of the flash memory or be loaded into the SHARC DSP from a host interface on reset when the flash memory needs to be reprogrammed. If placed in a read-only block, the routine is initially loaded into the SHARC DSP in the EPROM boot mode. It then checks an external program enable flag to decide whether to boot the currently programmed application or to enter the reprogramming mode. If the flag indicates the normal mode, the SHARC DSP skips over the reprogrammer routine and sets up a DMA from an address that is offset from 0x400000, which is the starting point of the application storage space.

Alternatively, a host can place the SHARC cluster in the host boot mode and perform a host boot of the reprogrammer routine into SHARC memory. This method frees up any boot blocks in the flash, at the expense of external circuitry to control the boot mode. The host will set the boot mode through a memory-mapped latch and reset the SHARC DSP for it to take effect. ❖

Distance Learning Package for EZ-KIT Lite

A self-paced distance learning package for the ADSP-2181 is now available from Northern Signal Processing Inc. The course covers all aspects of the use of the ADSP-2181 and the EZ-KIT Lite with emphasis on the device architecture, the peripherals, the memory interface, and the practical use of the full development tools. Each chapter of the course comes with a comprehensive tutorial section that exercises your grasp of the concepts and topics covered in that chapter. Each chapter also has a fully-tested suite of simulator and/or EZ-KIT Lite laboratory works so that you can gain experience in the use of these tools and the assembly language routines. A range of standard algorithms, like FIR and IIR filters and the Fast Fourier Transform are covered in detail.

The course costs $250.00 (US) and comes with a comprehensive suite of software examples and templates for the sim2181 software and the EZ-KIT Lite development system.

For further information, contact:

Northern Signal Processing Inc.
Suite 104
300, 8120 Beddington Blvd. N.W.
Calgary, AB, Canada T3K 2A8
Tel: (403) 275-9819
Fax: (403) 275-4261
Email: nsp_jim@agt.net ❖

Real-Time Kernel Library for SHARC DSP

Precision MicroDynamics Inc. announces Release 1.0 of LIBeRTy, a Real-Time Kernel Library for the ADSP-2106x family of DSPs. LIBeRTy provides a library of functions that extend the C Runtime Library to allow fast multitasking with low interrupt latency. This full-featured compact kernel uses only 4508 words of memory, leaving plenty of space for user code to reside on-chip. This makes LIBeRTy ideal for demanding embedded applications. LIBeRTy features a maximum interrupt latency of only 70 clock cycles and a semaphore/wait round-trip time (4 kernel calls + 2 context switches) of 791 clock cycles.

LIBeRTy is completely integrated with the Analog Devices DSP C environment. Programs are compiled with standard ADSP-2106x tools. By linking them with the kernel library, real-time multitasking capabilities can be realized. Facilities provided include task control (spawn, suspend, resume, abort), task synchronization via semaphores, and a message passing protocol. The kernel implements pre-emptive priority scheduling, plus a lower priority for the round robin execution of tasks.

Routines are provided for interface with a host computer. Source code is provided to demonstrate the use of the host interface with a BittWare ADSP-2106x board.

For complete information, contact:

Precision MicroDynamics Inc.
1961 Ferndale Road
Victoria, British Columbia,
Canada
V8N 2Y4
Tel: (604) 472-7249
Fax: (604) 472-1830
Email: info@pmdi.com
Internet: http://www.pmdi.com ❖

White Mountain DSP Development System for Sun Platform Supports SHARC DSPs

White Mountain DSP, Inc., a provider of DSP development tools, now supports Analog Devices' SHARC ADSP-2106x floating-point DSP family. Analog Devices and White Mountain DSP signed an agreement that brings SHARC emulation and debugging capability to Sun workstations. White Mountain DSP will develop and market the Mountain-ICE/WS SHARC emulator card for Sun SPARCstations and will provide support for both single-processor and multiprocessor debugging.

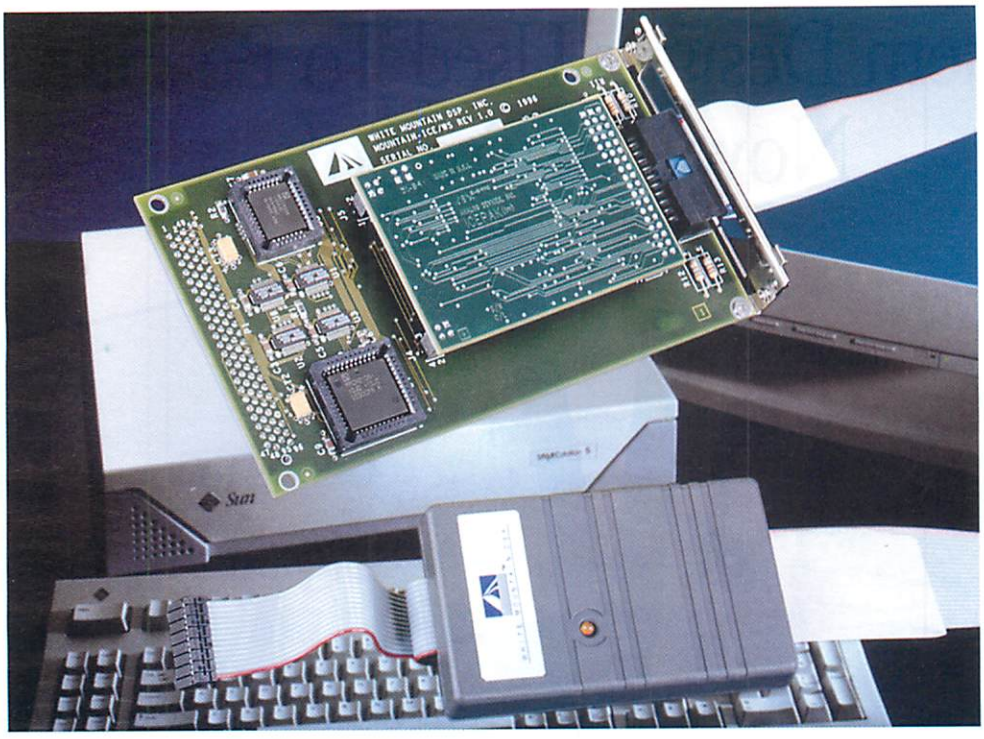
The release date for the Mountain-ICE/WS SHARC card, with uniprocessor and multiprocesor support, is set for October. The multiprocessor support gives developers the ability to launch multiple debugging sessions, facilitating synchronous lock-step control or discrete control of multiple SHARC DSPs in parallel-processing systems.

"Requests for SHARC DSP support have been frequent from all segments of the market in the past year," says White Mountain DSP's President, Peter Siy. "By providing developers with full-featured emulation and debugging capabilities, the Mountain-ICE/WS will speed the time to market of SHARC-based systems."

Features of the Mountain-ICE/WS for SHARC DSPs include:

- SBus-based emulation
- Supports both 3V and 5V devices
- Remote 3V and 5V emulator pod with cable
- Analog Devices' EZ-ICE debugger, running as an X Windows application under Open Windows version 3
- Support for SunOS 4.1x

In addition, White Mountain DSP will resell Analog Devices' ICEPAC emulator daughter card and probe



White Mountain DSP brings its emulation and debugger tools to SHARC DSPs.

card for SHARC target systems, making White Mountain DSP the first company to supply a complete SHARC development solution for Sun platforms. White Mountain DSP will also provide a SHARC version of the popular VISTA-MP multiprocessor debugger for Windows, called VISTA-ICE, scheduled for release early next year.

The August 1996 issue of White Mountain DSP's quarterly newsletter, DSP Summit, carried a full feature on the Mountain-ICE/WS. Subscriptions are free by e-mail: summit@wmdsp.com or call (603) 883-2430.

For more information, please contact:

White Mountain DSP, Inc.
410 Amherst Street, Suite 325
Nashua, NH 03063
Tel: (603) 883-2430
Fax: (603) 882-2655
Email: info@wmdsp.com
http:/www.techonline.com ❖

ADSP-2181-Based V.34 Modem Software

VoCAL Technologies, Ltd. offers complete V.34 modem software based on Analog Devices' family of fixed-point DSPs. The software fully supports 8 kHz sampling rates, the standard data rate used in most digital telephony systems. Typical applications include modems for embedded designs, such as security systems, PBXs, ISDN terminal adapters, Internet access devices, dial-up routers, channel bank modems, and telephony on T1 and E1 (European standard) lines.

A single general-purpose ADSP-2181 is used for all the modem modulations specified by the ITU (formerly the CCITT) and other telephony functions such as DTMF generation and call progress detection.

Direct acceptance of 8 kHz data allows digital telephony products using VoCAL's software to couple modem capabilities seamlessly with digital telephony trunks and lines. Keeping the functionality in software gives the customer the ability to offer future upgrades and compatibility with emerging standards. Using the ADSP-2181 means not only that customers don't need special chips to implement their designs, but also that products can be upgraded in the field simply by downloading new software.

OEMs can customize the software for a particular hardware configuration or use it with VoCAL's low-cost, royalty-free reference design. It is offered as individual modules, as a complete suite or as part of a turnkey hardware-software solution. VoCAL provides comprehensive integration and support services.

VoCAL telephony software is available immediately, for a fixed fee of $25,000 to $350,000 or on a per-unit royalty basis.

For more information, contact:

VoCAL Technologies Ltd.
1576 Sweet Home Road
Buffalo, NY 14228
Tel: (716) 688-4675
Fax: (716) 636-3630
Email: info@vocal.com
www.analog.com/ADSP2181 ❖

Modem Designs Used To Be Hard. Now They're Soft.

ADSP-2181: A Single Chip With The DSP, Memory And Peripherals To Run A Range Of Embedded Modem Algorithms.

Whether you're working on an embedded modem for Internet access, PBXs or ISDN terminal adapters, keeping up with evolving standards and end-user features isn't hard anymore. The ADSP-2181 DSP gives you the flexibility of a RAM-based processor plus the benefit of a high-speed architecture. With a 24-bit instruction word and 16-bit data word, the ADSP-2181 performs in applications from V.34 fax/modems to G.728 speech compression.

	ADSP-2181 MIPS	Low Cost External Memory	Download File Size
Network Access V.34, V.32bis	20	0	148 KB
Network Access V.34, V.32bis, V.42, V.42bis, MNP 2-5	25	32 K x 24 35 nsec access time	191 KB
ISDN Terminal Adapter V.34, V.32bis, V.17	21	0	160 KB
DSVD Modem 4, V.32bis, G.729A	30	32 K x 24 35 nsec access time	175 KB
x Modem V.17	6.5	0	26 KB
Embedded Modem V.32bis	11.5	0	30 KB
Full-Duplex Speakerphone	9.5	0	32 KB
G.728 LD-CELP	28	0	24 KB

Special Code-Swapping Capability

The ADSP-2181 has unique features to facilitate gram segment overlay. For example, your DSP receive a call with its answering machine code loaded, swap to V.8 protocol code when it hears a modem signal, then swap to V.34 code when it determines the modulation required. In addition, an 8-bit Byte DMA lets you overlay and download from low-cost external memory.

Reprogramming And Upgrades Are Easy

The need to patch code, add new features and support new telecom standards necessitates modem reconfigurability. The ADSP-2181 makes it simple with 80 KBytes of SRAM on-chip. Not only can you change the code, you can also change the program memory/data memory partitioning. FLASH memories or ROM can't do that. In addition, DMA support and a simple host interface mean that initializing the memory just got easy.

On-chip telecom-compatible peripherals allow you to move high-speed data from telephony lines and network servers in/out of the ADSP-2181 without wasting MIPS interrupting your core algorithm execution.

One IC Bridging LAN To WAN

The ADSP-2181 also provides telecom-compatible peripherals on-chip. Like a 16-bit host IDMA port that acts as a high-speed data and control interface to the server or backbone. A multichannel serial port that connects directly to T1, E1 and other telephony lines. And DMA that eliminates the need to interrupt the processor while data transfers in/out.

So be hard on your competition. Work with Analog Devices and our third party solution providers for your next design.

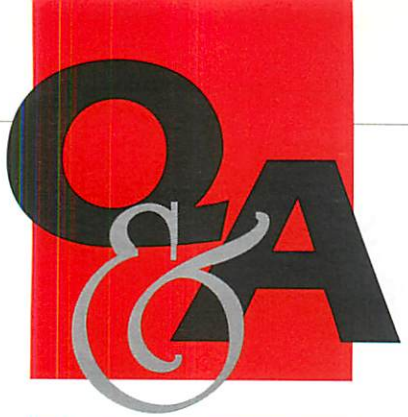
For ADSP-2181 technical information call 1-800-ANALOGD (262-5643)†, or visit us on the World Wide Web at: http://www.analog.com/ADSP2181 to learn more about the ADSP-2181 in modem designs.

/www.analog.com

ANALOG DEVICES
Analog. Digital. Solutions.

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106.
Distribution, offices and application support available worldwide.

† Outside U.S., please call 617-461-3392.



Q ADSP-2181 Memory Access Priorities

I have an ADSP-2181-based design which uses the IDMA port and the serial port. I am doing IDMA and SPORT Autobuffer transfers simultaneously and would like to know which transfer has priority—IDMA or SPORT Autobuffer?

The ADSP-2181 evaluates the priority of latched requests on every cycle.

A *If you are doing simultaneous IDMA and SPORT Autobuffer transfers, IDMA transfers have priority. If a SPORT Autobuffer request happens first, followed very shortly by another SPORT Autobuffer request and an IDMA transfer, the first Autobuffer request will be serviced, and then the DSP will evaluate the priority of all latched requests and perform the IDMA transfer.*

In general, whichever transfer request occurs first gets serviced, but the DSP evaluates the priorities of latched requests on every cycle. It does not queue the requests in the order they arrived. ❖

Q Memory Configuration of the ADSP-21csp01

I have designed my project using an ADSP-21xx family processor and now I am ready to port it to the newer ADSP-21csp01 processor. How does the memory configuration of the ADSP-21csp01 differ from the memory configuration of the ADSP-21xx family?

With the ADSP-21csp01, Program memory and data memory share a single, unified 16M word space.

A *The memory configuration of the ADSP-21csp01 is significantly different from the memory configuration of the ADSP-21xx family.*

The ADSP-21csp01 has a total of 24 address lines for accessing to up to 16M words of memory space. Program memory and data memory are no longer separate memory spaces; rather there is now a single unified memory space. PM now refers to a 24-bit access, and DM now refers to a 16-bit memory access. The internal memory of the ADSP-21csp01 is divided into four 2K blocks. Two of the blocks are 24 bits wide and are available for instructions and data. The other two blocks are for data storage only and are 16 bits wide.

The memory map of the ADSP-21csp01 is evenly divided into four banks of 4M words each. External to the device, banks are selected by the MS[3:0] memory select pins. MS[3:0] pins are determined by the two MSBs of the address. An external I/O space with its own select line has been added to the ADSP-21csp01.

The data and I/O spaces are paged. The memory space for data accesses is divided into 256 64K word pages. There are four page registers used for data accesses. The eight MSBs of the 24-bit address buses are driven by one of the four page registers and the 16 LSBs are driven from the instruction DAG or DMA controller. The selection of which of the four registers used is implicit in the instruction type. DAG1 and immediate instructions use DMPG1; DAG2 instructions

use DMPG2; the (DMAPAGE) register is used for DMA/Host Interface port transfers; and the (SPORTPAGE) register is used for serial port transfers. I/O space accesses use the IOPG page register.

The program counter is 24 bits wide, therefore program sequencing does not require paging. To the program sequencer, the unified memory space is a 16M word linear program space. The only case where a programmer must set a page register for program flow control is when doing an indirect jump using the DAGs. The IJPG register is used to indicate what memory page to jump to. ❖

Q Conditional Jumps on the ADSP-21csp01

In my ADSP-21xx design, I use the instruction: `IF POS JUMP label;` now I see that the if POS and if NEG instructions are not listed in the ADSP-21csp01 Programmer's Quick Reference. What instructions can I use in their place?

With the ADSP-21csp01, 4-bit condition codes are specified in the condition code register (CCODE).

A *The ADSP-21xx family condition codes for ALU X Input Sign Negative and ALU X Input Sign Positive (AS status bit) have been replaced in the ADSP-21csp01 by a programmable condition code (CCODE) register.*

The condition code register (CCODE) is a 4-bit register used for programming the new software condition codes.

Conditional Instructions COND

CCODE	1010	1011
0x00	FLAGIN0 HI	FLAGIN0 LO
0x01	FLAGIN1 HI	FLAGIN1 LO
0x02	FLAGIN2 HI	FLAGIN2 LO
0x03	FLAGIN3 HI	FLAGIN3 LO
0x04	FLAGIN4 HI	FLAGIN3 LO
0x05	FLAGIN5 HI	FLAGIN3 LO
0x06	undefined	undefined
0x07	underfined	underfined
0x08	X input NEG	X input POS
0x09	SV	not SV
0x0a-0x0f	underfined	underfined

The following ADSP-21xx family instructions,

```
IF POS JUMP label_1;
IF NEG JUMP label_2;
```

will be replaced by the following ADSP-21csp01 instructions:

```
CCODE = 8;                    /* check X input sign */
IF SWCOND JUMP label_1;       /* jump to label_1 if POS */
IF NOT SWCOND JUMP label_2;   /* jump to label_2 if NEG */
```

The CCODE register is also used to check FLAGIN conditions and shifter overflow.

Note: *The CCODE register defaults to 0x08 on reset.* ❖

Writing a C Program for a SHARC DSP

In previous installments of C Tips, we focused on writing efficient C programs for the ADSP-2100 family of fixed-point processors. In this issue, we'll begin to take a look at some useful tips for writing a C program for the SHARC floating-point DSP.

All the programs described here were written with the ADDS-210XX-SW-PC release 3.2 development software and have been tested on the ADDS-2106x-EZ-LAB. There are some restrictions regarding the software tools so please read the release notes.

Writing an Architecture File

An architecture file, *.ACH, is used to describe the target system on which your C program will run. Two examples are available on the Analog Devices DSP BBS and can be used to give you a quick start: 21062C.ACH could be used to run C code on the EZ-LAB, and the 21060c.ACH is for those who have upgraded their EZ-LAB with an ADSP-21060. The CINIT, CSTACK, and CHEAP directives are used only for C programming and are described in the ADSP-21000 Family C Tools Manual. If you want to divide up your memory in another way, refer to chapter 5 of the ADSP-2106x SHARC User's Manual.

Putting C Functions in Alternative Segments

Sometimes you may want to place C functions in a different segment from the default segment, seg_pmco. You can do that easily with the g21k compiler.

In the following example, the main program, sum.c, calls the external function, ext.c, in the alternative code segment alt_pmco.

```
/* This program calls an
external C function in an
alternative code segment */
extern int sum(int a,int b);
void main(void)
{
/* - VAR - */
int i=5;
int j=3;
/* - MAIN - */
i= sum(i,j);
idle();
}
/* PRG END */
```

The external functions could look like the following code:

```
int sum(int a, int b)
{
return a+b;
}
```

To compile this example, use the command lines:

```
g21k sum.c -c -a 21062c.ach
g21k ext.c -c -mpmcode=alt_pmco
g21k sum.o ext.o -a 21062c.ach
-o sum -map -g
```

The -mpmcode switch chooses the alternative code segment. Variables placed in the data memory (dm) or program memory (pm) space could be put in an alternative segment by invoking the compiler with a similar switch:

```
-mdmdata, -pmdata
```

Extensions to ANSI C

The Analog Devices C compiler supports ANSI C. Nevertheless there are some extensions that are very useful. Since you can store data in either the program or the data memory of the SHARC, an additional keyword indicates where the linker is to place variables. Use the PM directive to place variables in program memory and the DM directive to place them in data memory—for example:

```
float dm source(16)
float pm dest(16)
```

When no directive is given, the linker will place the variable in the data memory by default. The default memory segment in which the dm variables are placed is labeled seg_dmda, and the default segment for variables that reside in program memory is called seg_pmda.

Often it is useful to place the variables in different segments—for example external memory space. An easy way to do that is to use the include file named macros.h delivered with the package. To use this file, add the directive:

```
#include<macros.h>
```

to your source code and use the following syntax:

```
DEF_VAR (name, type, seg, mem)
where:
name = variable name
type = the actual C type
seg = the segment in the
architecture file
mem = the memory in which the
variable exists, either pm or
dm
```

Another useful macro is called DEF_PORT. This macro, which has the same syntax as the previous directive, can be used to define an I/O port in C:

The necessary segment declaration in the architecture file could look like the following line:

```
.SEGMENT /PORT /
BEGIN=0x00404000 /
END=0x00404000 /DM /width=32
mafeadrs;
```

It is worthwhile to look at the macros.h file, as it contains a lot of useful declarations that are not yet documented. Additional extensions are described in the ADSP-21000 Family C Tools Manual, chapter 5.

Accessing IOP Registers

Most of the SHARC's control registers are memory-mapped to the address range 0x0000 to 0x0100. To access these memory-mapped IOP registers, use the following syntax in your C code:

```
#define        SYSCON
*(int*)0x000
```

Using this pointer assignment allows you to change the content of the System Control register in the C file with the following instruction:

```
SYSCON = 0x1234;
```

The header file, def06xc.h, already defines some IOP registers. This file must be included at the beginning of your program to allow this convenient way of accessing IOP control registers. The syntax is:

```
#include<def06xc.h>
```

Embedded Assembly Language

The core processor system registers (MODE1, MODE2, ASTAT, STKY, IRPTL, IMASK, IMASKP, USTAT1, and USTAT2) are not memory-mapped. Therefore they cannot be accessed using the syntax above. They can be modified only by using the in-line assembler feature:

```
asm("1st instruction;
2nd instruction;
:
last instruction;");
```

To be able to manipulate the bits of these registers easily, include the def21060.h header file at the beginning of your in-line assembler code:

```
asm("#include<def21060.h>;
bit set imask LP2I;
bit set mode1 IRPTEN;");
```

Any other assembler instruction can be placed within the "asm();" directive.

The syntax shown above can be used to place any valid assembler instruction within your C source code. Inserting assembler instructions is very useful if you want to have a minimum of overhead—for time-critical program sections.

You can also call assembler routines out of the main C program. The procedure is described in detail in chapter 4 of the ADSP-21000 Family C Tools Manual.

```
/* File main.c calls external asm
subroutine mul2 to multiply two
numbers */
extern float mul2(float x, float
y);
main()
{
        float a = 0.25;
        float b = 0.75;
        float c;
        c = mul2(a,b); /* call
assembler subroutine */
idle();
exit(0);
```

```
/* File extmul.asm */
#include<asm_sprt.h>
.segment/pm    seg_pmco;
.global          _mul2;
_mul2:
leaf_entry;
f0=f4*f8; /* fetch first and
second parameter */
leaf_exit;
.endseg;
```

If you want to call external assembler subroutines or functions from the main C code, the easiest way to link the two programming languages is to invoke the g21k compiler as follows:

```
g21k file1.c file2.asm
-a 21062c.ach -o out.exe
```

In this way you don't have to care about how to invoke the linker ld21K.

Compiling C Code

After you write your C code, the compiler should be invoked in the following way:

```
g21k code.c -a 21062C.ach
-o output -g
```

The -g switch is used to generate debuggable code for the simulator and emulator. If you want the compiler to produce optimized code, use one of the following switches:

```
-O, -O2, -O3
```

Remember, however, that you can't use the CBUG feature for code that has been optimized. Furthermore, the iterators (ITER) of the numerical C extension do not work with the -O3 switch. Using any optimization switch often causes the following problem: If a variable is checked in a loop but is not updated in that loop, the compiler removes the test of the variable from the loop to minimize the number of instructions. That could cause errors when the value of this variable is updated within an interrupt service routine and should be evaluated in the main loop. To avoid this problem, you must declare the variable as volatile:

```
volatile int test_flag;
```

In future installments of C Tips, we will discuss the programming of interrupts, link port DMA and other useful elements. ❖

Up To Date

GSM Cellular Phone Solution

Analog Devices and The Technology Partnership (TTP) now offer the first commercially available chip set and software combination to have survived the arduous Global System for Mobile Communications (GSM) type approval process. For the first time, you can develop cellular-phone handsets with the confidence that your products will meet the stringent performance requirements of the European Telecommunications Standards Institute (ETSI).

Since 1993 Analog Devices has been teamed with TTP, Cambridge, England, to create a complete chip set (ADSP-21msp410) and software solution for baseband signal processing for GSM phones. By adopting this proven solution, you can reduce GSM phone development times by a year or more. Other chip suppliers can claim hardware working in GSM phones, but only Analog Devices and TTP can show a type-approved hardware and software combination. ❖

Sound Controllers Add Audio and Telephony Mixing to Games

Analog Devices expands its line of single-chip sound controllers by delivering CD-quality fidelity and five channels of digital mixing for the cost of a SoundBlaster-only game audio IC. The AD1815 integrates a V.34 modem front end and targets motherboards. The AD1816 integrates 3D audio effects processing and targets add-in card designs. Both provide the signal-processing hardware to complement MMX instruction-based audio and telephony capabilities in PCs.

Both the AD1815 and the AD1816 include a stereo 16-bit sigma-delta audio codec; support for voice-over data applications; full-duplex capture and playback operation at different sample rates; the ability to convert, mix, and synchronize up to six different sample rates simultaneously; an integrated music synthesizer with documented compatibility for SoundBlaster applications; Plug and Play compatibility and integrated PnP ROM; and Windows®95 drivers. The AD1815 and AD1816 sound controllers are packaged in 100-pin PQFPs. ❖

Wavelet Video Compression IC

Analog Devices is the first company to implement wavelet-based video compression in silicon. The ADV601 Video Codec supports 10-bit lossless compression/decompression of broadcast-resolution digital video (CCIR-601). The chip integrates video and host interfaces with on-chip SRAM to minimize the need for external devices and reduce system cost. One key application for the part is the PC video capture and editing market, where it enables the lowest system cost ever available for Super VHS-quality desktop video production. The low cost and professional features of the ADV601 also make it suitable for many other real-time encoding applications.

The ADV601 is packaged in a 160-pin PQFP and priced at $35.95 in quantities of 10,000 units.

Advantages of Wavelets

Symmetry, scalability, precision, and error tolerance are key advantages of wavelet mathematics that benefit a variety of signal-processing applications, including video processing and communications. The symmetry of wavelets means the silicon required for encoding is virtually the same as the silicon required for decoding, making the cost of encoding and decoding equal.

Scalability means the bit stream can be edited on-the-fly and scaled for viewing at whatever resolution and frame rate the target system or transmission channel can support.

Wavelet technology also features an error-tolerant bit stream. The compressed data representing a frame contains information about the entire image, not simply a block of pixels within the image, as with images compressed using JPEG or MPEG. Lost data does not result in lost blocks within the image, and the entire image can be reconstructed from the error-free data. ❖

ADSP-2181 IDMA Application Note

Are you planning a host-based design with the ADSP-2181? If so, check out a new application note entitled ADSP-2181 IDMA Interface to Motorola MC68300 Family of Microprocessors. Although the MC68300 family is used as the example interface, this application note provides useful information applicable to a host-to-IDMA port interface design using other popular microprocessors.

Topics covered in this application note include IDMA operation, hardware interface design, DSP boot code generation, and host download issues. Also included are hardware interface design schematics, sample host source code, and source code for a utility program that converts DSP executable files to an IDMA port compatible format.

Obtain the application note by requesting it from ADI's literature center, or find it on the Analog Devices Internet home page at http://www.analog.com under the heading of Technical Support. ❖

New DSP Products to be Unveiled at DSP World

Analog Devices will be introducing a number of new DSP products at the International Conference on Signal Processing Applications & Technology (ICSPAT) featuring DSP World, which will be held in Boston at the World Trade Center from October 7-10. If you have preregistered for the show, be sure to look for our mailing which details key events for the week. You can preregister by contacting ICSPAT/DSP World at (214) 446-1367. For the latest in DSP, visit Analog Devices at Booth #870. ❖

ADSP-2100/21000 Family Workshop Schedule

The ADSP-2100 Family and ADSP-21000 Family Workshops are a fast way to get started designing with Analog Devices' DSPs. The workshops last three days and include hands-on lab sessions where you'll work with the hardware and software development tools available to support your design effort.

To register, place an order with your local Analog Devices Sales Office or Distributor for the System Development &Programming With The ADSP-2100 Family workshop (part# ADDS–21XX–WKSHP) or System Development &Programming With The ADSP-21000 Family workshop (part# ADDS–210XX–WKSHP), and call the site contact listed below in the schedule to give us your registration information. Class size is limited to facilitate maximum individual instruction and practical hands-on experience.

Upcoming workshops are scheduled for the following dates and locations.

- Atlanta, Georgia
  Oct. 2-4, 1996 (2100 Family)
  Nov. 6-8, 1996 (21000 Family)
  Jan. 15-17, 1997 (2100 Family)
  To register, contact Gordon Cooper at (770) 497-4440
- Campbell, California
  Nov. 6-8, 1996 (2100 Family)
  Dec. 11-13, 1996 (21000 Family)
  To register, contact Colin Duggan at (408) 879-3037
- Norwood, Massachusetts
  Sept. 18-20, 1996 (2100 Family)
  Oct. 23-25, 1996 (21000 Family)
  Dec. 11-13, 1996 (2100 Family)
  Jan. 15-17, 1997 (21000 Family)
  To register, contact Nelia Elias at (617) 461-3672 or (617) 461-3881
- St. Louis, Missouri
  Sept. 18-20, 1996 (21000 Family)
  To register, contact Greg Geerling at (314) 921-4429

Current Software Releases

Product	Latest Release
ADSP-2100 Family Development Software	5.1
ADSP-21000 Family Development Software	3.2
ADSP-21cspxx Family Development Software	Beta Test
ADSP-2101 EZ-LAB	EPROM 1.4
ADSP-2111 EZ-LAB	EPROM 1.4
ADSP-2171 EZ-LAB	1.0
ADSP-21020 EZ-LAB	2.0 (H/W)
ADSP-2106x EZ-LAB	3.11 (S/W); 3.0 (FW); 3.0 (H/W)
ADSP-21cspxx EZ-LAB	Beta Test
ADSP-2101 EZ-ICE	5.01
ADSP-2111 EZ-ICE	5.01
ADSP-2171 EZ-ICE	5.01
ADSP-2181 EZ-ICE	5.11
ADSP-21020 EZ-ICE	3.2
ADSP-2106x EZ-ICE	3.22

Each release of the software is shipped with a Release Note. This note describes the current version and provides information on any upgrades to the software. Please be sure to return the registration card enclosed with your shipment! This allows us to keep you informed of subsequent releases.

Available Literature

Circle corresponding numbers on the enclosed reply card to request items of interest. The numbers appearing in parenthesis correspond to our Faxcode numbers.

Data Sheets

1 ADSP-2100 Family DSP Microcomputers† (1579)
2 ADSP-2104/ADSP-2109 Low Cost DSP Microcomptuter (2050)
3 ADSP-2171/72/73 DSP Microcomputer (1869)
4 ADSP-2181 DSP Microcomputer (1927)
5 ADSP-21msp58/59 DSP Microcomputer (1901)
6 ADSP-21060/62 SHARC (1870)
7 ADSP-21csp01 Concurrent Signal Processor (Preliminary) (1975)
8 ADSP-2100 Family Development Tools (1919)
9 ADSP-21000 Family Development Tools (1489)
10 ADV601 Low Cost Multiformat Video Codec (Preliminary) (2011)
11 AD1815 Sound Codec (1987)
12 AD1816 Sound Codec (2029)

Application Notes

13 Selecting a DSP Processor (ADSP-2115 vs. TMS320C5x)
14 Selecting a DSP Processor (ADSP-2181 vs. TI & Motorola)
15 Selecting a DSP Processor (ADSP-21060 vs. TMS320C40)
16 ADSP-2181 IDMA Interface to Motorola MC68300 Family of Microprocessors

Special

17 Digital Signal Processing Brochure
18 System Development & Programming with ADSP-2100 & ADSP-21000 Families Workshop Brochure
19 EZ-KIT Lite Brochure
20 DSP/MSP Products Reference Manual

Manuals

(Manuals must be ordered through your local sales office.)

- ADSP-2100 Family User's Manual (Order with part number ADSP-21XX-USERS-ML)
- ADSP-21020 User's Manual
- ADSP-2106x SHARC User's Manual
- ADSP-2100 Family EZ TOOLS Manual (Order with part number ADSP-21XX-EZ-MAN)
- ADSP-2100 Family Assembler Tools & Simulator Manual (Order with part number ADSP-21XX-DSW-ML)
- ADSP-2100 Family C Tools Manual (Order with part number ADSP-21XX-CTOOL-ML)
- ADSP-2100 C Runtime Library Reference (Order with part number ADSP-21XX-CRTL-MAN)
- ADSP-21000 Family Assembler Tools & Simulator Manual (Order with part number ADSP-210XX-DSW-MAN)
- ADSP-21000 Family C Tools Manual (Order with part number ADSP-210XX-CTOOLML)
- ADSP-21000 C Runtime Library Reference (Order with part number ADSP-210XX-CRTL-ML)
- Digital Signal Processing Applications Using the ADSP-2100 Family (Prentice Hall), Vol. 1 (Order with part number ADSP-21XX-APPS-BK1)
- Digital Signal Processing Applications Using the ADSP-2100 Family (Prentice Hall), Vol. 2 (Order with part number ADSP-21XX-APPS-BK2)
- ADSP-21000 Family Applications Handbook, Vol. 1

† This data sheet combines and replaces the following individual data sheets: ADSP-2101, ADSP-2103, ADSP-2105, ADSP-2111, ADSP-2115, and the ADSP-216x.

DSPatch® is published by the Computer Products Division of Analog Devices. It is created and edited by the Applications Group to aid those using or considering Analog Devices DSP components.

DSPatch welcomes comments, letters and articles on topics of interest to those designing digital signal processing and related high-performance systems. We will publish submitted articles that are of broad interest.

Additional copies are available from your local Analog Devices Sales Office. Address all correspondence to:

DSPatch
Analog Devices, Inc.
Computer Products Division
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106

You may also contact the Computer Products Division:

- *By contacting your local Analog Devices Sales Representative*
- *For Marketing and Applications Engineering information, call 1-800-ANALOG-D*
- *The Norwood office Fax number is (617) 461-3010*
- *The Norwood office may also be reached by email at cpd_support@analog.com*

DSP Bulletin Board Service (617) 461-4258

8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud

Internet FTP Site

Type: ftp ftp.analog.com or ftp 137.71.23.21
Login as anonymous using your email address for your password

DSP Applications Assistance Line (617) 461-3672

Call weekdays 8:00 a.m. to 5:00 p.m. Eastern Time
Technical Assistance can also be obtained in Europe by fax at ++49-89-57005-200 or email at dsp.europe@analog.com
Technial Assistance is also available from Analog Devices Authorized Distributors

AnalogFax™ Automated Literature Delivery System 1-800-446-6212

Visit Us on the World Wide Web at http://www.analog.com

G2153-72-9/96